**W1kHz Clock Divider**

module clk\_div\_kh(

input clk,

output reg clk\_khz);

reg [8:0] counter;

initial begin

counter = 9'b000000000;

clk\_khz = 0;

end

always @ (posedge clk) begin

counter <= counter + 1'b1;

if(counter == 500) begin

counter <= 0;

clk\_khz <= ~clk\_khz;

end

end

endmodule

**1Hz Clock Divider**

module clk\_div\_h(

input clk,

output reg clk\_hz);

reg [25:0] counter;

initial begin

counter = 26'b0;

clk\_hz = 0;

end

always @ (posedge clk) begin

counter <= counter + 1'b1;

if(counter == 50000000) begin

counter <= 0;

clk\_hz <= ~clk\_hz;

end

end

endmodule